Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A chip-packaging with bonding options connected to a package substrate, comprising:

a package substrate;

a chip mounted on the package substrate, the chip comprising a plurality of bonding pads, one of the bonding pads being connected to the package substrate; and

a lead frame connected to one of the bonding pads.

[c2] 2.The chip-packaging in the claim 1, wherein the package substrate is connected to a high voltage or a low voltage.

[c3] 3.The chip-packaging in the claim 2, wherein the high voltage is a power supply and the low voltage is ground.

[c4] 4.The chip-packaging in the claim 1, wherein the lead frame is connected to a pin of the chip.

[c5] 5.The chip-packaging in the claim 4, wherein the pin is connected to a high voltage, a low voltage, or an input/output signal.

[c6] 6.A method of packaging a chip having a bonding option

connected to a package substrate, comprising:

providing the package substrate;

mounting the chip on the package substrate, the chip comprising a plurality of bonding pads;

connecting one of the bonding pads to the package substrate; and

connecting one of the bonding pads to a lead frame.

[c7] 7.The method of packaging a chip in claim 6 further comprising connecting the package substrate to a high voltage or a low voltage.

[c8] 8.The method of packaging a chip in claim 7, wherein the high voltage is a power supply of the chip, and the low voltage is ground of the chip.

[c9] 9.The method of packaging a chip in claim 6 further comprising connecting the lead frame to one pin of the chip.

[c10] 10.The method of packaging a chip in claim 9 further comprising connecting the pin to a high voltage, a low voltage, or an input/output signal.